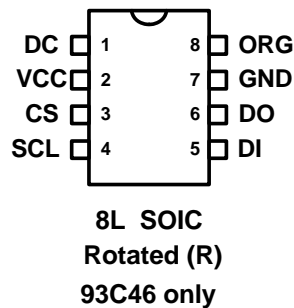
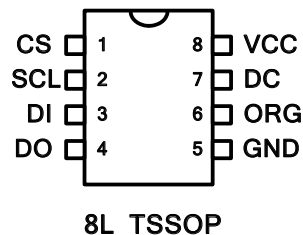
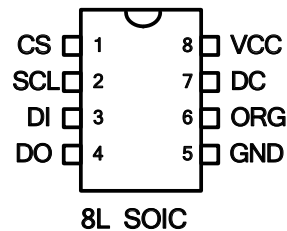
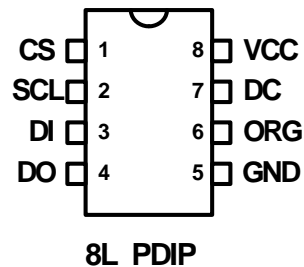


PIN CONFIGURATION

Pin Name	Pin Function
CS	Chip Select
SCL	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
ORG	Internal Organization
DC	Don't Connect
VCC	Power Supply
GND	Ground

All these packaging types come in Pb-free certified.



ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40°C to 85°C
Storage temperature:	-50°C to 125°C
Input voltage on any pin relative to ground:	-0.3V to $V_{CC} + 0.3V$
Maximum voltage:	8V

* Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.

MEMORY ORGANIZATION

The FT93C46/56/66 memory is organized either as bytes (x8) or as words (x16). If Internal Organization (ORG) is unconnected (or connected to VCC) the words (x16) organization is selected; When Internal Organization is connected to ground the bytes (x8) organization is selected.

INSTRUCTION SET for the FT93C46

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A ₆ - A ₀	A ₅ - A ₀			Reads data stored in memory, at specified address.
EWEN	1	00	11xxxxxx	11xxxx			Write enable must precede all programming modes.
EWDS	1	00	00xxxxxx	00xxxx			Disables all programming instructions.
ERASE	1	11	A ₆ - A ₀	A ₅ - A ₀			Erase memory location A _n - A ₀ .
WRITE	1	01	A ₆ - A ₀	A ₅ - A ₀	D ₇ - D ₀	D ₁₅ - D ₀	Writes memory location A _n - A ₀ .
ERAL	1	00	10xxxxxx	10xxxx			Erases all memory locations.
WRAL	1	00	01xxxxxx	01xxxx	D ₇ - D ₀	D ₁₅ - D ₀	Writes all memory locations.

INSTRUCTION SET for the FT93C56 and FT93C66

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A ₈ - A ₀	A ₇ - A ₀			Reads data stored in memory, at specified address.
EWEN	1	00	11xxxxxxxx	11xxxxxxxx			Write enable must precede all programming modes.
EWDS	1	00	00xxxxxxxx	00xxxxxxxx			Disables all programming instructions.
ERASE	1	11	A ₈ - A ₀	A ₇ - A ₀			Erase memory location A _n - A ₀ .
WRITE	1	01	A ₈ - A ₀	A ₇ - A ₀	D ₇ - D ₀	D ₁₅ - D ₀	Writes memory location A _n - A ₀ .
ERAL	1	00	10xxxxxxxx	10xxxxxxxx			Erases all memory locations.
WRAL	1	00	01xxxxxxxx	01xxxxxxxx	D ₇ - D ₀	D ₁₅ - D ₀	Writes all memory locations.

(A) START BIT (SB)

Each instruction is preceded by a rising edge on Chip Select (CS) with Serial Clock (SCL) being held Low.

(B) OPERATION CODE (OP-CODE)

Two op-code bits, read on Serial Data Input (DI) during the rising edge of Serial Clock (SCL).

(C) ADDRESS

The address bits of the byte or word that is to be accessed. For the FT93C46, the address is made up of 6 bits for the x16 organization or 7 bits for x8 organization. For the FT93C56, the address is made up of 7 bits for the x16 organization or 8 bits for x8 organization. For the FT93C66, the address is made up of 8 bits for the x16 organization or 9 bits for x8 organization.

(D) DATA

The data bits of the byte or word that is to be accessed. For the FT93C46/56/66, the data is made up of 16 bits (word) for the x16 organization or 8 bits (byte) for x8 organization.

INSTRUCTION SETS DESCRIPTION

(A) READ

The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that when a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.

(B) ERASE/WRITE ENABLE

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

(C) ERASE/WRITE DISABLE

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

(D) ERASE

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

(E) WRITE

The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP} , starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP} .

(F) ERASE ALL

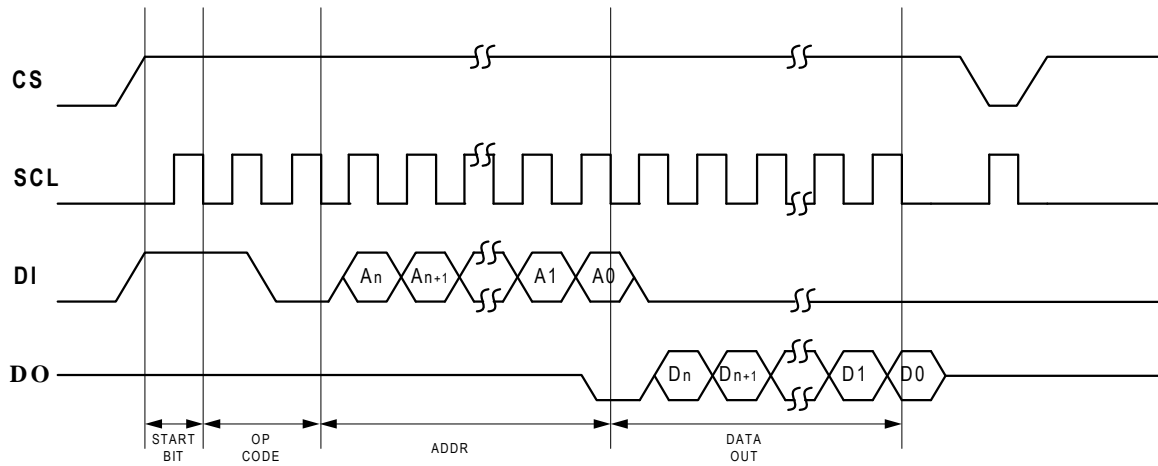
The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

(G) WRITE ALL

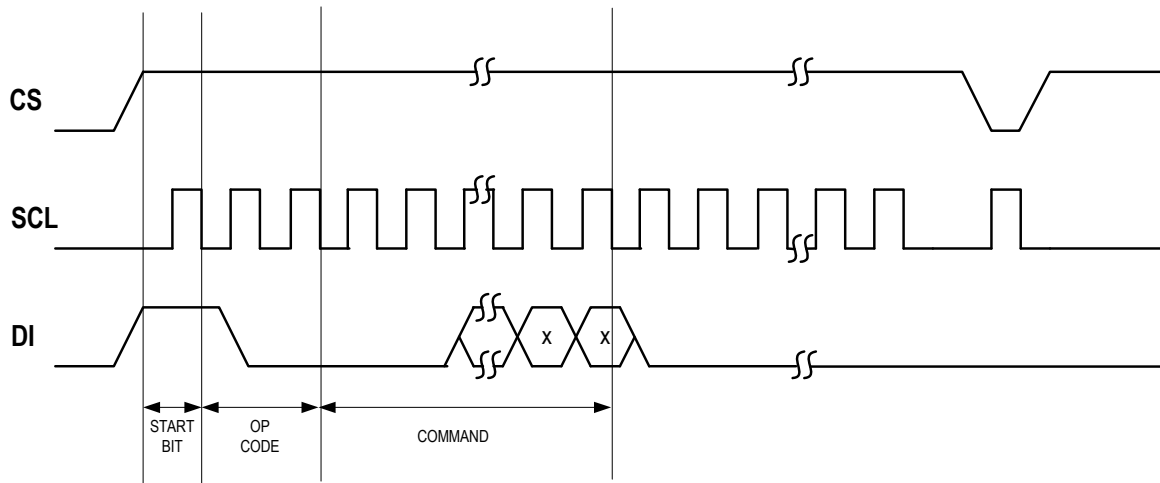
The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0V \pm 10\%$.

Timing Diagrams

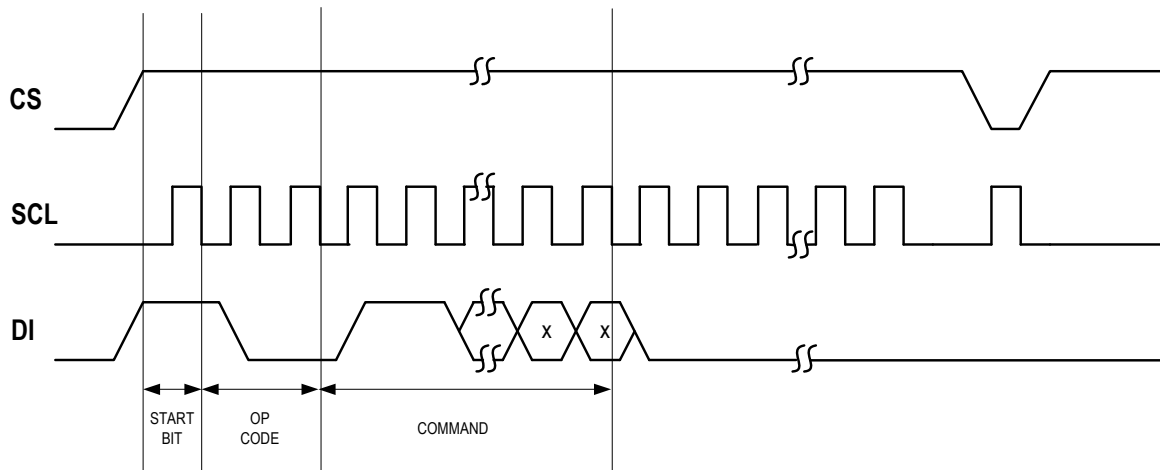
READ Timing



EWDS Timing

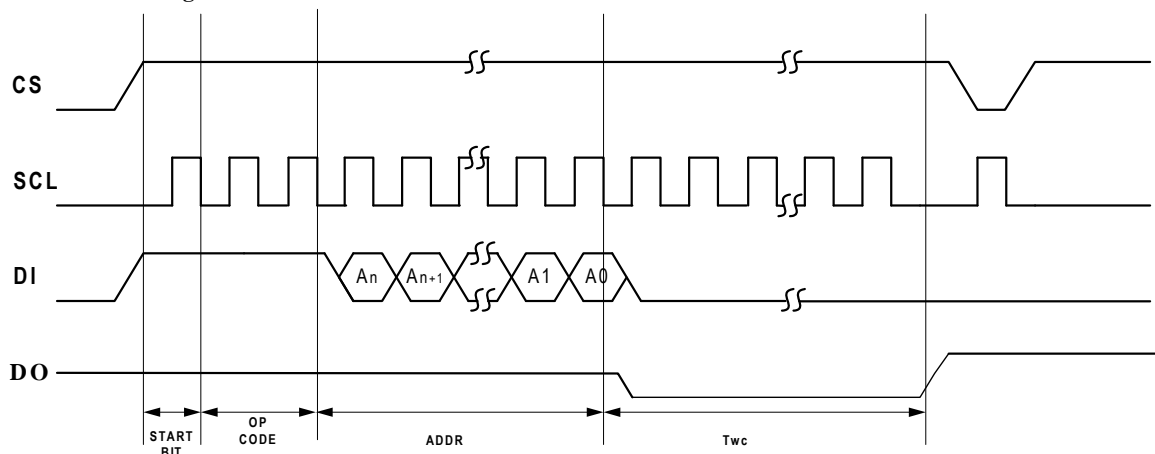


EWEN Timing

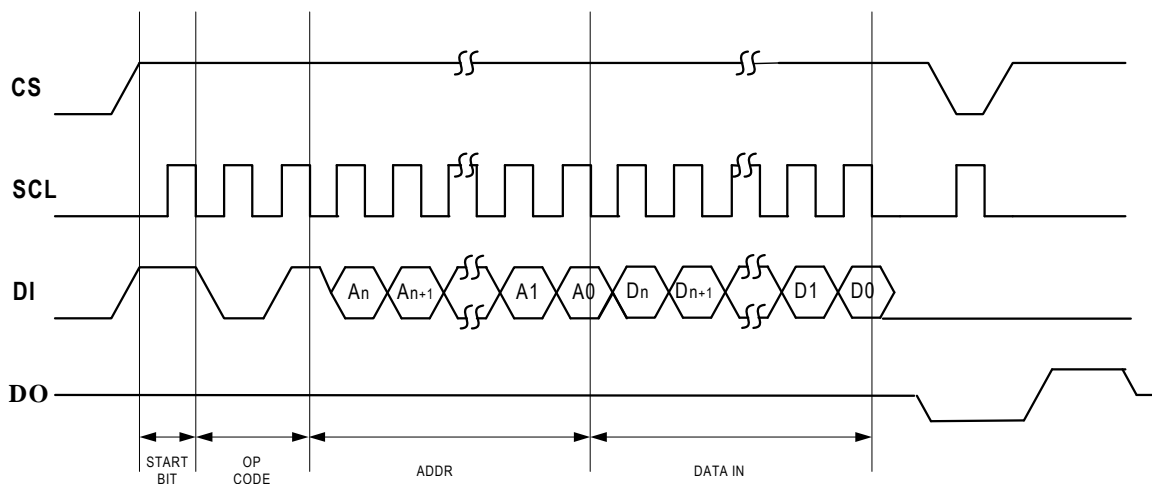


93C46/A, 93C56/A, 93C66/A

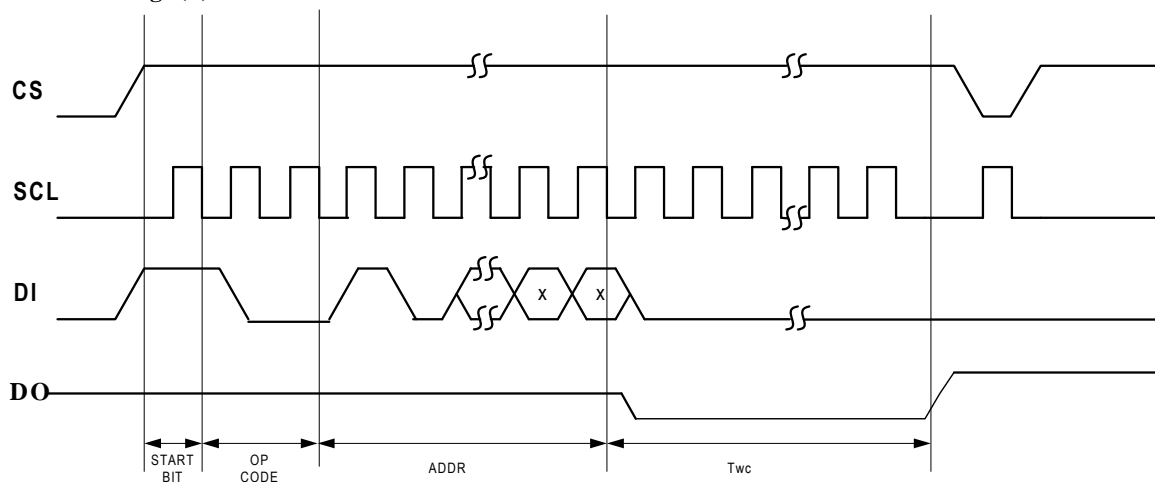
ERASE Timing



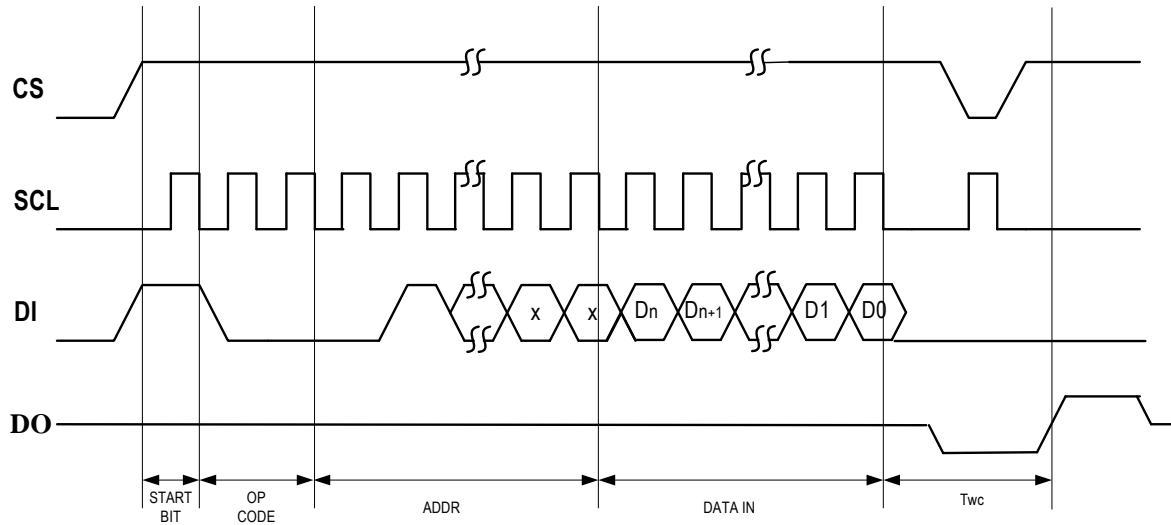
WRITE Timing



ERASE Timing (1)

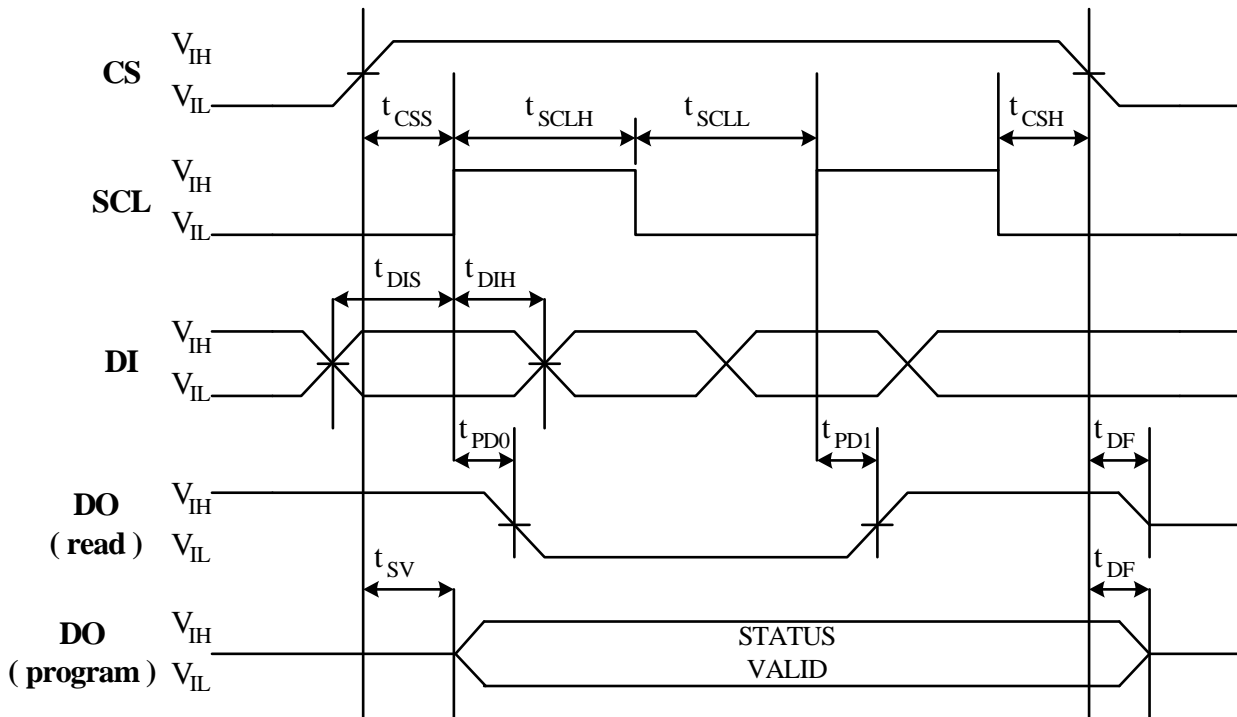


WRAL Timing (2)



- Note : 1. Valid only at $V_{CC}=4.5V$ to $5.5V$
 2. Valid only at $V_{CC}=4.5V$ to $5.5V$

Synchronous Data Timing



93C46/A, 93C56/A, 93C66/A

AC CHARACTERISTICS

Applicable over recommended operating range from: $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	0 0 0		2 1 0.25	MHz
t_{SCLH}	SCL High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
t_{SCLL}	SCL Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
t_{CS}	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
t_{CSS}	CS Setup Time	Relative to SCL	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	50 50 200		ns
t_{DIS}	DI Setup Time	Relative to SCL	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100 400		ns
t_{CSH}	CS Hold Time	Relative to SCL	0			ns
t_{DIH}	DI Hold Time	Relative to SCL	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100 400		ns
t_{PD1}	Output Delay to '1'	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		250 250 1000	ns
t_{PD0}	Output Delay to '0'	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		250 250 1000	ns
t_{SV}	CS to Status Valid	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		250 250 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		100 100 400	ns
t_{WC}	Write Cycle Time		$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	3	10	ms

93C46/A, 93C56/A, 93C66/A

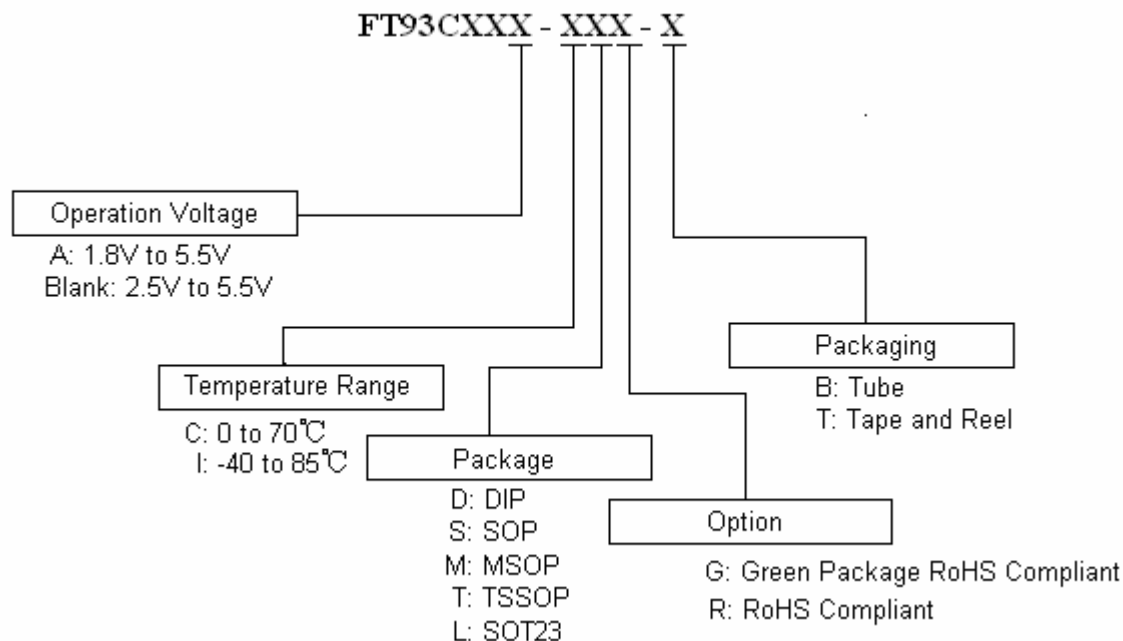
DC CHARACTERISTICS

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1$ TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.8\text{V}$	$CS = 0\text{V}$		0	0.1	μA
I_{SB2}	Standby Current	$V_{CC} = 2.5\text{V}$	$CS = 0\text{V}$		6.0	10.0	μA
I_{SB3}	Standby Current	$V_{CC} = 2.7\text{V}$	$CS = 0\text{V}$		6.0	10.0	μA
I_{SB4}	Standby Current	$V_{CC} = 5.0\text{V}$	$CS = 0\text{V}$		17	30	μA
I_{IL}	Input Leakage	$V_{in} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
I_{OL}	Output Leakage	$V_{in} = 0\text{V}$ to V_{CC}			0.1	1.0	μA
$V_{IL1}^{(1)}$ $V_{IH1}^{(1)}$	Input Low Voltage Input High Voltage	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6 2.0		0.8 $V_{CC} + 1$	V
$V_{IL2}^{(1)}$ $V_{IH2}^{(1)}$	Input Low Voltage Input High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		-0.6 $V_{CC} \times 0.7$		$V_{CC} \times 0.3$ $V_{CC} + 1$	V
V_{OL1}	Output Low Voltage		$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OH1}	Output High Voltage	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OH} = -0.4\text{ mA}$	2.4			V
V_{OL12}	Output Low Voltage		$I_{OL} = 0.15\text{ mA}$			0.2	V
V_{OH2}	Output High Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$			V

93C46/A, 93C56/A, 93C66/A

ORDER CODE:



ORDER INFORMATION

Order code	Vcc	Temperature Range	Package	Option	Packaging	PIN
FT93C46A-CDG-B	1.8v-5.5v	0-70°C	DIP8	Green Package	Tube	
FT93C46A-CDR-B	1.8v-5.5v	0-70°C	DIP8	RoHS	Tube	
FT93C46A-IDG-B	1.8v-5.5v	-40-85°C	DIP8	Green Package	Tube	
FT93C46A-IDR-B	1.8v-5.5v	-40-85°C	DIP8	RoHS	Tube	
FT93C46-CDG-B	2.5v-5.5v	0-70°C	DIP8	Green Package	Tube	
FT93C46-CDR-B	2.5v-5.5v	0-70°C	DIP8	RoHS	Tube	
FT93C46-IDG-B	2.5v-5.5v	-40-85°C	DIP8	Green Package	Tube	
FT93C46-IDR-B	2.5v-5.5v	-40-85°C	DIP8	RoHS	Tube	
FT93C46A-CSG-B	1.8v-5.5v	0-70°C	SOP8	Green Package	Tube	
FT93C46A-CSG-T	1.8v-5.5v	0-70°C	SOP8	Green Package	T/R	
FT93C46A-CSR-B	1.8v-5.5v	0-70°C	SOP8	RoHS	Tube	
FT93C46A-CSR-T	1.8v-5.5v	0-70°C	SOP8	RoHS	T/R	
FT93C46A-ISG-B	1.8v-5.5v	-40-85°C	SOP8	Green Package	Tube	
FT93C46A-ISG-T	1.8v-5.5v	-40-85°C	SOP8	Green Package	T/R	
FT93C46A-ISR-B	1.8v-5.5v	-40-85°C	SOP8	RoHS	Tube	
FT93C46A-ISR-T	1.8v-5.5v	-40-85°C	SOP8	RoHS	T/R	
FT93C46-CSG-B	2.5v-5.5v	0-70°C	SOP8	Green Package	Tube	
FT93C46-CSG-T	2.5v-5.5v	0-70°C	SOP8	Green Package	T/R	
FT93C46-CSR-B	2.5v-5.5v	0-70°C	SOP8	RoHS	Tube	

